REMARKS

Claims 1-15 are pending in the application. Claims 1-15 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Kwak (U.S. Pat. No. 6,667,792). Specifically, the Examiner states that "Kwak discloses a digital DLL apparatus for use in a semiconductor memory device operating in synchronization with an external clock, comprising: a frequency-detecting unit (figure 3, direct phase detector 350) that receives the external clock (ext_clk), detects clock frequency information of the external clock, and outputs the detected clock frequency information (detector 350 outputting the detected clock frequency information to the delay line unit 320); and a duty cycle correction circuit that corrects the duty cycle of the external clock in response to the clock frequency information (Figure 3, delay line unit 320 incorporated with blend circuit 330 correcting the frequency of the external clock to synchronize with internal clock based on the detecting signal; col. 5, lines 29+)."

Contrary to the Examiner's assertions, the digital DLL apparatus disclosed in Kwak does not detect or use the ***frequency*** of the external clock to perform a duty cycle correction. Rather, Kwak teaches the use of ***phase*** detectors and a blending circuit to "generat[e] a blended clock signal having 50% duty cycle by blending ***phases*** of the first delayed internal clock signal and second delayed internal clock signal in case that rising edges of the first clock signal and second clock signal are matched identically." Col. 2, lines 59-64 (emphasis added). The direct phase detector 350 is a phase detector, not a frequency detector. A phase detector detects phase information; a frequency detector detects frequency information. Kwak does not teach any use of frequency information for controlling the digital DLL.

As shown and described in the present application, the phase detectors and the frequency detecting unit are not the same and provide different functions. *See, e.g.*, Application, Fig. 5 (showing phase detectors 502, 512 and frequency detecting unit 5200) and pp. 6-9 (explaining different functions of phase detectors 502, 512 and frequency detecting unit 5200). For example, as described with respect to the embodiment shown in Fig. 5, the phase detectors control the variable delay lines 501, 511, while the frequency detecting unit 5200 is used to control the capacitances of capacitors in an interpolation circuit 520. *See* Application, pp. 7-8.

For these reasons, claim 1 and each of its dependent claims (2-5) are believed to be patentable over the prior art of record.

The dependent claims are also patentable, however, for additional reasons. With respect to claims 3 and 4, for instance, Kwak does not even teach the use of capacitors in its blend circuit 330, let alone controlling the capacitance of the capacitors in response to clock frequency information. Furthermore, with respect to claim 5, there is no mention in Kwak of an analog to digital converter for converting frequency information into a digital signal.

The Examiner rejected claims 6-8, 9-11, and 12-15 on the same grounds as claims 1-5 without performing a separate analysis. Claims 6-15 are therefore believed patentable for the reasons discussed above with respect to claims 1-5 and other reasons.

For the foregoing reasons, reconsideration and allowance of claims 1-15 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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I hereby certify that this correspondence is being transmitted to the U.S. Patent and Trademark Office via facsimile number (703) 872-9306 on January 31, 2005.

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